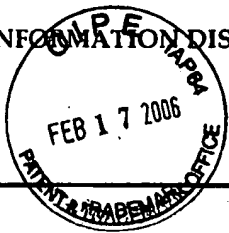


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INFORMATION DISCLOSURE STATEMENT				APPLICANT: Fitzgerald			
				SERIAL NO.: 10/774,890			
				FILING DATE: February 9, 2004 GROUP: 2818			
U.S. PATENT DOCUMENTS							
EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A191	5,091,767	02/25/1992	Bean et al.			
	A192	5,571,373	11/05/1996	Krishna et al.			
	A193	5,633,202	05/27/1997	Brigham et al.			
	A194	5,710,450	01/20/1998	Chau et al.			
	A195	5,976,939	11/02/1999	Thompson et al.			
	A196	6,876,053	04/05/2005	Ma et al.			
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EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)						
	C135	Abstreiter et al., "Silicon/Germanium Strained Layer Superlattices," <u>Journal of Crystal Growth</u> , 95:431-438 (1989).					
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	C137	Cao et al., "0.18-μm Fully-Depleted Silicon-on -Insulator MOSFET's," <u>IEEE Electron Device Letters</u> , 18(6):251-253 (1997).					
	C138	Chau et al., "Advanced CMOS Transistors in the Nanotechnology Era for High-Performance, Low-Power Logic Applications", pp. 26-30 (2004).					
	C139	Eichinger et al., "Characterization of MBE Growth SiGe Superlattices with SIMS and RBS, <u>Proceedings of the First International Symposium on Silicon Molecular Beam Epitaxy</u> , 85(7):367-375 (1985).					
	C140	Fair, "Concentration Profiles of Diffused Dopants in Silicon," <u>Impurity Doping Processes in Silicon</u> , Chapt. 7, pp. 318-442 (1981).					
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INFORMATION DISCLOSURE STATEMENT		APPLICANT:	Fitzgerald
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OTHER ART, JOURNAL ARTICLES, ETC.			
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)		
	C144	Gibbons et al., "Limited reaction processing: Silicon epitaxy", <u>Appl. Phys. Lett.</u> , 47(7):721-723 (1985).	
	C145	Godbey et al., "A Si _{0.7} Ge _{0.3} Strained Layer Etch Stop for the Generation of Bond and Etch Back SOI", <u>IEEE SOS/SOI Tech. Conf. Proc.</u> , p. 143-144 (1989).	
	C146	Gronet et al., "Growth of GeSi/Si strained-layer superlattices using limited reaction processing", <u>J. Appl. Phys.</u> , 61(6):2407-2409 (1987).	
	C147	Hobart et al., "Ultra-Cut: A Simple Technique for the Fabrication of SOI Substrates with Ultra-Thin (<5 nm) Silicon Films", <u>Proceedings 1998 IEEE International SOI Conference</u> , pp. 145-146 (1998).	
	C148	Holländer et al., "Reduction of Dislocation Density of MBE-Grown Si _{1-x} Ge _x Layers on (100) Si by Rapid Thermal Annealing", <u>Thin Solid Films</u> , 183:157-164 (1989).	
	C149	Huang et al., "SiGe-on-insulator prepared by wafer bonding and layer transfer for high-performance field-effect transistors", <u>Appl. Phys. Lett.</u> , 78(9):1267-1269 (2001).	
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	C151	Ismail, et al., "Extremely high electron mobility in Si/SiGe modulation-doped heterostructures", <u>Appl. Phys. Lett.</u> , 66(9):1077-1079 (1995).	
	C152	Ismail, et al., "Gated Hall effect measurements in high-mobility n-type Si/SiGe modulation-doped heterostructures", <u>Appl. Phys. Lett.</u> , 66(7):842-844 (1995)	
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	C158	Noble et al., "Reduction in misfit dislocation density by the selective growth of Si _{1-x} Ge _x /Si in small areas", <u>Appl. Phys. Lett.</u> , 56(1):51-53 (1990).	
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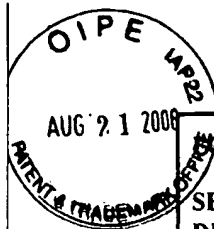
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INFORMATION DISCLOSURE STATEMENT		APPLICANT: Fitzgerald
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	C159	Schäffler et al., "Letter to the Editor, High-electron-mobility Si/SiGe heterostructures: influence of the relaxed SiGe buffer layer", <u>Semicond. Sci. Technol.</u> , 7:260-266(1992).
	C160	Shifren et al., "Drive current enhancement in p-type metal-oxide-semiconductor field-effect transistors under shear uniaxial stress," <u>Appl. Phys. Lett.</u> , 85(25):6188-6190 (2004).
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	C164	Taraschi et al., "Relaxed SiGe-on-insulator fabricated via water bonding and etch back," <u>J. Vac. Sci. Technol. B</u> , 20(2):725-727 (2002).
	C165	Taraschi et al., "Strained-Si-on-Insulator (SSOI) and SiGe-on-Insulator (SGOI): Fabrication Obstacles and Solutions," <u>Mat. Res. Soc. Symp. Proc.</u> , 745:105-110 (2003).
EXAMINER		DATE CONSIDERED



FORM PTO - 1449				ATTY DOCKET NO.: ASC-049C1			
SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT				APPLICANT: Fitzgerald			
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				FILING DATE: February 9, 2004			
				EXAMINER: Tran, Mai Huong C.			
				GROUP: 2818			
U.S. PATENT DOCUMENTS							
EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
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EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)						
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	C167	Ming et al., "Interfacial roughness scaling and strain in lattice mismatched Si _{0.4} Ge _{0.6} thin films on Si" Applied Physics Letters, Vol. 67, No. 5, July 31, 1995, pp. 629-631.					
	C168	Ming et al., "Microscopic structure of interfaces in Si _{1-x} Ge _x /Si heterostructures and superlattices studied by x-ray scattering and fluorescence yield," Physical Review B, Vol. 47, No. 24, pp. 373-81, June 15, 1993.					
	C169	Nishi et al. "Handbook of Semiconductor Manufacturing Technology," Marcel Dekker AG, New York, NY, 2000, pp. 1-22					
	C170	O'Neill, et al., "Deep Submicron CMOS Based on Silicon Germanium Technology," <i>Fellow</i> , IEEE Transactions on Electron Devices, Vol. 43, No. 6, June 1996 pp. 911-918.					
	C171	Sugii, et al., "Role of Si _{1-x} Ge _x buffer layer on mobility enhancement in a strained-Si channel metal-oxide-semiconductor field-effect transistor," <u>Central Research Laboratory</u> , Hitachi Ltd. 1-280 Higashi-Koigakubo, Kokubunji-shi, Tokyo 185-8601 Japan, pp. 2948-2950.					
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